

TRANSMITTAL OF INFORMATION DISCLOSURE STATEMENT
(Under 37 CFR 1.97(b) of 1.97(c))

Docket No.
BUR920030123US1

In Re Application Of: **Gray et al.**

FEB 20 2004



Serial No.

10/707,287

Filing Date

12/03/03

Examiner

Unassigned

Group Art Unit

Unassigned

Title: **CIRCUIT AREA MINIMIZATION USING SCALING**

Address to:

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

37 CFR 1.97(b)

1. ☒ The Information Disclosure Statement submitted herewith is being filed within three months of the filing of a national application other than a continued prosecution application under 37 CFR 1.53(d); within three months of the date of entry of the national stage as set forth in 37 CFR 1.491 in an international application; before the mailing of a first Office Action on the merits, or before the mailing of a first Office Action after the filing of a request for continued examination under 37 CFR 1.114.

37 CFR 1.97(c)

2. ☐ The Information Disclosure Statement submitted herewith is being filed after the period specified in 37 CFR 1.97(b), provided that the Information Disclosure Statement is filed before the mailing date of a Final Action under 37 CFR 1.113, a Notice of Allowance under 37 CFR 1.311, or an Action that otherwise closes prosecution in the application, and is accompanied by one of:
- ☐ the statement specified in 37 CFR 1.97(e);
- OR**
- ☐ the fee set forth in 37 CFR 1.17(p).

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Payment of Fee

(Only complete if Applicant elects to pay the fee set forth in 37 CFR 1.17(p))

- ☐ A check in the amount of _____ is attached.
- ☒ The Director is hereby authorized to charge and credit Deposit Account No. 09-0456 (IBM) as described below.
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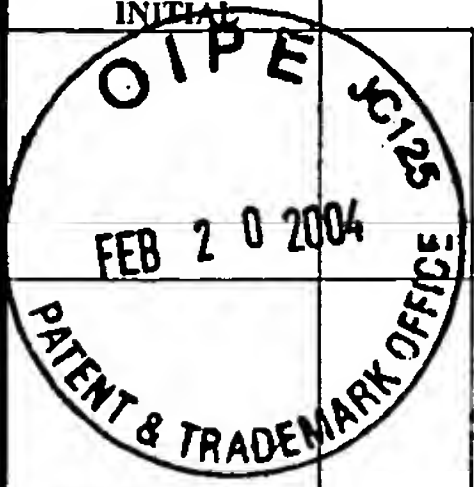
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INFORMATION DISCLOSURE CITATION (Use several sheets if necessary)		Docket Number (Optional) BUR920030123US1	Application Number 10/707,287
		Applicant(s) Gray et al.	
		Filing Date 12/03/2003	Group Art Unit Unassigned
*EXAMINER INITIAL	OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)		
	"Process Independent Constriant Graph Compaction," D. Boyer, 29th ACM/IEEE Design Automation Conference, Paper 21.4, pp. 318-322.		
	"An Algorithm to Compact a VLSI Symbolic Layout with Mixed Constraints," Y. Z. Liao et al., 20th Design Automation Conference, Paper 9.1, IEEE, 1983, pp. 107-112.		
	"Graph-Optimization Techniques for IC Layout and Compaction," G. Kedem et al., 20th Design Automation Conference, Paper 9.2, IEEE, 1983, pp. 113-120.		
	"Symbolic Layout Compaction Review," D. Boyer, 25th ACM/IEEE Design Automation Conference, Paper 26.1, 1988, pp. 383-389.		
	"A Subjective Review of Compaction," Y. Cho, 22nd Design Automation Conference, Paper 25.1, IEEE, 1985, pp. 396-404.		
	"An Introduction to VLSI Physical Design," M. Sarrafzadeh et al., Chapter 7, "Compaction," Section 7.1.2, "Graph-based Techniques," McGraw-Hill (1996), pp. 276-279.		
	"Algorithms for VLSI Physical Design Automation," 3rd Edition, N. Sherwani, Chapter 12, "Compaction," Section 12.3.1, "Constraint-Graph based Compaction," Kluwer Academic Publishers (1999), pp. 453-463.		
EXAMINER		DATE CONSIDERED	
*EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP Section 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.			